ADS8344/45 EVM User's Guide

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1 Introduction

The ADS8344 and ADS8345 are complete 16-bit analog-to-digital (A/D) using state-of-the-art CMOS structures. They contain a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D with sample-and-hold, external reference, and a serial data interface. Programmable options allow the use of an internal oscillator or the external serial clock as the conversion clock source.

The EVM is available with either the ADS8344 and ADS8345 installed. The EVM can accommodate the 12-bit ADS7844 by simply removing and replacing the installed device. Samples of the ADS7844 can be obtained through the sample program at Texas Instruments. See the ADS7844 Product Folder for details.

1.1 Features

- Full-featured Evaluation Board for the ADS8344 or ADS8345, serial Analog to Digital Converters
- 5V Analog Input Range
- Built in reference
- High-Speed Serial Interface
- Compatible with the 5-6K Interface Card for use with a variety of DSP Starter Kits as well as the HPA-MCU Interface for use with C2000 and TMS470 processors.
- Field Programmable Gate Array (FPGA) users can evaluate the ADS8344/45 EVM by obtaining the Texas Instruments Analog Adapter Kit from Avnet Design Services (www.em.avnet.com).

2 Analog Interface

For maximum flexibility, the ADS8344/45 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at P1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 shows the pin out of the analog input connector, J1.

Table 1. Pinout of the Analog Input Connector, P1

Pin Number	Signal	Description
P1.2 thru P1.16 (even)	Analog Input	The eight analog inputs are applied to the even pins of P1. CH7 is configured via jumper W1 to use either the on-board amplifier U1 or the R/C filter combination of R17 and C25.
P1.20	REF(+)J	External reference source input, accessible through W5.
P1.15	REFOUT	Not connected on this EVM
P1.1- P1.19 (odd)	AGND	Analog ground connections.

The analog front-end (AFE) circuitry for channels 0-6 found on the EVM consists of a simple RC filter. When used in combination with the 5-6K Interface Board, the circuits found on both DAP Signal Conditioning Boards (see SLAU105) provide the level shifting and amplifier configurations to realize single ended or bi-polar mode operation of the analog-to-digital converter installed on the EVM.

2.1 Amplifier Input to CH7

Jumper W1 provides access to an amplifier/buffer circuit on the front end of the data converter. Component U1, an OPA132, is installed on the EVM by default and is configured as a simple voltage follower. Any standard 8 pin SOIC single amplifier component can be installed at this location to explore the tradeoffs of speed and performance when interfacing to the ADC.

The amplifier circuit is connected to the ±VA terminals for split supply operation. If single supply amplifiers are used, the –VA (J3 pin 2) can be tied to analog ground using jumper W4. When used in conjunction with the 5-6K Interface Board, be aware that the –VA supply is common to all power connectors (JP1 through JP6). Shorting the –VA supply to ground on the ADS8344/45 EVM is possible only if it is not used elsewhere on the interface board.

3 Digital Interface

The ADS8344/45 EVM is designed for easy interfacing to multiple control platforms. Jumper options are provided on the EVM to allow direct control over the chip select source and the BUSY signal output.

The active low $\overline{CS}$ pin is connected to the center terminal of W8. Pins 1 and 3 of W8 connect to P2 pins 1 and 7 respectively. This allows the /CS line to be controlled through GPIO functions on the 5-6K Interface Board or the HPA-MCU, as well as through the Frame Sync function of various TI DSP's. For stand alone operation, a shunt jumper can be placed between P2 pins 1 and 2 of W8 to tie $\overline{CS}$ to ground.

The DATA output from the EVM is applied to P2 pin 13. The BUSY output can be applied to either P2.9 or P2.15 to act as an external interrupt to the host processor, or the Frame Sync return input to 5000 and 6000 series DSPs.

3.1 Additional Digital Control and Monitoring

W2 controls the device power down function. Closing W2 applies a logic low to the SHDN pin, shutting down the ADC. W2 can be wired to GPIO output P2 pin 19 for use with the HPA-MCU board.

Wire loops W6 and W8 provide access to the BUSY and /CS signals respectively. These can be monitored by referencing an oscilloscope to P2.18, which connects to digital ground.

4 Power Supplies

The ADS8344/45 EVM board requires +5V DC for the analog and +3.3 – +5V DC for the digital sections of the board. Power to the ADC is sourced from J3 pin 3. Power for the digital section of the board is sourced from J3 pin 9 or 10 via wire jumper W7. The positive supply voltage to the amplifier at U1, U4 and the reference at U3 are provided via J3 pin 1. The negative supply for amplifier U1 is provided by J3 pin 2.

Note: Use caution when applying power to the EVM.

The following table shows the pin out of J3:

Table 2. Pinout of J3

Signal	Pin Number		Signal
+VA	1	2	-VA
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

For stand alone operation, power sources can be applied via various test points located on the EVM (VANA to TP2 and VDIG to TP3). Refer to the schematic at the end of this document for details.

Note: While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

4.1 Reference Voltages

The ADS8344/45 is normally configured to use its on-board reference source. Jumper W5 provides options to allow the EVM user to send the voltage output from U3 or the external reference applied to P1.20 through buffer amplifier U4. U4 is always in circuit – to bypass U4, resistor R7 can be removed from the circuit.

5 EVM Operation

Once power is applied to the EVM, the analog input source can be connected directly to P1 (top or bottom side) or through optional amplifier and signal conditioning modules using the 5-6K Interface Board or HPA-MCU Interface Boards.

The digital control signals can be applied directly to P2 (top or bottom side). The ADS8344/45 EVM can also be connected directly to the 5-6K Interface Board for use with a variety of C5000 and C6000 series DSP Starter Kits (DSK). The analog and digital input connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1" centers.

No specific evaluation software is provided with this EVM, however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments. Check the product folders or send e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are available on request.

Table 3 shows the factory default jumper locations for the ADS8344/45 EVM:

Table 3. Factory Default Jumper Locations

Jumper	Function	Default Condition
W1	Controls application of the applied analog signal to CH7	1–2
W2	Controls application of the DC level to SHDN pin	Open
W3	Controls application of the applied +VA to input amplifier	1–2
W4	Controls application of the applied -VA to input amplifier	1–2
W5	Controls the application of the reference voltage	1–2
W6	Controls the output location of the BUSY signal - INT (default) or FSR	1–2
W7	Controls the application of digital I/O voltage	1–2
W8	Controls the application of the /CS Source	1–2

6 EVM Bill of Materials and Schematic

Table 4 contains a complete Bill of Materials for the ADS8344/45EVM. The schematic diagram is also provided for reference.

Table 4. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1 C2 C3 C13 C14 C15 C16 C18 C21 C26	0.1µF, Ceramic, X7R, 25V	TDK	C2012X7R1E104K
C4 C6 C11 C12 C19 C20	10µF , Ceramic, 0805, 16V	Murata	GRM21BR61C106KE15L
C7 C8 C9 C10 C22 C23 C24 C25	680 pF, Ceramic, 0603, 50V	TDK	C1608C0G1H681J
C17	0.47µF, Ceramic, 0603, X5R, 10V	TDK	C1608X5R1A474K
C27	22µF, Ceramic, 0805, Y5V, 6.3V	TDK	C2012Y5V0J226Z
C28	0.01µF, Ceramic, 0805, COG, 16V	AVX	0805YA103JAT2A
C5	Not Installed		
P1 P2 (top side)	10 pin, dual row, SMTheader (20 pos.)	Samtec	TSM-110-01-T-DV-P
J1 J2 (bottom side)	10 pin, dual row, SMT socket (20 pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (bottom side)	5 pin, dual row, SMT socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
FB1 FB2 FB3 FB4	Ferrite Chip, 120 Ω, 200mA, 1206	TDK	MZA3216D121C
R2 R8	0Ω , 0603	Yageo America	9C06031A0R00JLHFT
R3 R4 R5 R6 R14 R15 R16 R17	200 Ω, 0603, 5%	Yageo America	9C06031A2000JLHFT
R7	100 Ω, 0603, 5%	Yageo America	9C06031A1000JLHFT
R9 R20 R21	10K Ω, 0603, 5%	Yageo America	9C06031A1002JLHFT
R10 R11 R12	1K Ω, 0603, 5%	Yageo America	9C06031A1001JLHFT
R13 R22 R23	10 Ω, 0603, 5%	Yageo America	9C06031A10R0JLHFT
R18 R19	0 Ω, 0603 - Depending on U2 - See the Schematic	Yageo America	9C06031A0R00JLHFT
TP1 TP2	Black test point loop	Keystone	5001
U1	OPA132	TI	OPA132U
U2	ADS8344 or ADS8345	TI	ADS8344E or ADS8345E
U3	REF3240	TI	REF3240AIDBVR
U4	OPA364	TI	OPA364AIDBVR

Table 4. Bill of Materials (continued)

Designators	Description	Manufacturer	Mfg. Part Number
U5 U6	SN74LVC1G07	TI	SN74LVC1G07DBVR
W1 W3 W4 W5 W6 W7 W8	3 pin , 0.1" header	Samtec	TSW-103-07-L-S
W2	2 pin , 0.1" header	Samtec	TSW-102-07-L-S

7 Related Documentation from Texas Instruments

Table 5. EVM Compatible Device Data Sheets, Users Guides and Additional Resources

Data Sheet	Literature Number
ADS8344	SBAS139
ADS8345	SBAS177
ADS7844	SBAS100
Users Guides	**Literatuare Number**
5-6K Interface Board	SLAU104
DAP Signal Conditioning Boards	SLAU105
Additional Resources	**Literature Number**
Op Amps for Everyone	SLOD006

Revision History		
REV	ECN Number	Approved
C	6434958_SCH_RC	TH

TP2
R1 Not Installed
C5 Not installed
AGND
R2 0R
+VA
C2 0.1uF
-In
+In
Output
U1
B_CH3
W1
CH7a
CH7
-VA
C1 0.1uF
P1
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
REFP
R5 200
R6 200
R4 200
R3 200
C9 680pF
C8 680pF
C7 680pF
C10 680pF
Note:-
Plug is installed topside (P)
Socket is installed bottomside (J)
R14 200
R15 200
R16 200
R17 200
C22 680pF
C23 680pF
C24 680pF
C25 680pF
+Vcc_A
C16 0.1uF
C26 0.1uF
U2
ADS8344/5
CH0_LPF
CH1_LPF
CH2_LPF
CH3_LPF
CH4_LPF
CH5_LPF
CH6_LPF
CH7_LPF
+Vcc
CS*
DCLK
Din
DOUT
BUSY
SHDN*
VREF
COM
GND
BCLK
R13 10
R11 1K
R10 1K
R9 10K
R18* 0R
R19* 0R
C19 10uF
C15 0.1uF
W2
R20 10K
U6
U5
SN74LVC1G07
+Vcc_D
W8
W6
INT
CS
CLKx
BCLK
FSx
FSr
DX
DR
P2
R21 10K
Note:-
Plug is installed topside (P)
Socket is installed bottomside (J)
* Note:
R19 is installed for ADS8344 EVM's
R18 is installed for ADS8345 EVM's
+3.3VD
W7
FB4
+Vcc_D
C21 0.1uF
C20 10uF
+5VA
FB3
+Vcc_A
C13 0.1uF
C12 10uF
C11 10uF
W3
+VA
FB1
+Vs_A
C3 0.1uF
C4 10uF
J3
+Vs
-Vs
DGND
AGND
+5VD
FB2
-Vs_A
C14 0.1uF
C6 10uF
W4
-VA
TP1
R8 0R
AGND
DGND
+Vcc_A
U3
REF32XX
IN
ENA
GNDS
OUTS
GNDF
OUTF
C17 0.47uF
R22 10
C27 22uF
REFP
W5
R23 10
U4
OPA364N
C18 0.1uF
R7 100R
VREF+
C28 10nF
R12 1K

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Title:	ADS8344/8345 Evaluation Module
Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	ADS8344_45 Rev C
DOCUMENTCONTROL #	6434956
REV:	C
DATE:	15-Jan-2007
SIZE:	
SHEET:	1 OF: 1

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 15 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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